WHAT IS CLAIMED IS:

1. A function reconfigurable semiconductor device, comprising:

a plurality of function cells, each of said function cells being a basic unit which realizes a function;

each of said function cells including a plurality of threshold elements;

each of said threshold elements including means which stores a threshold value; and

wherein a function which is realized by said function cell is determined by determining said threshold value in each of said threshold elements.

2. The semiconductor device as claimed in claim 1, further comprising a nonvolatile memory which stores data for realizing said function in said function cells.

3. The semiconductor device as claimed in claim 2, wherein said function cells are connected by wiring which can change a connection status.

4. The semiconductor device as claimed in claim 3, further comprising at least two control systems,

each of said threshold elements being

connected to said control systems via said wiring; and

at least one control system of said control systems being connected to said nonvolatile memory.

5. The semiconductor device as claimed in claim 1, each of said function cells including a plurality of stages, each of said stages including at least one threshold element.

6. The semiconductor device as claimed in claim 5, each of said threshold elements comprising:

a first input part which inputs an input signal to be processed;

a second input part which inputs a control signal for realizing said function;

wherein said threshold value is set by said control signal, an output value for an input signal which is input from said first input part being determined according to said threshold value.

7. The semiconductor device as claimed in claim 5, each of said threshold elements comprising:

a plurality of input terminals;

a first terminal which can be regarded as in an electrically insulated state transiently; and

a nonlinear element;

said input terminals being connected to said first terminal; and

said nonlinear element receiving a voltage of said first terminal.

8. The semiconductor device as claimed in claim 7, each of said threshold elements further comprising:

a first switch between said first terminal and a terminal having a first predetermined voltage;

at least one second switch being connected to at least one input terminal of said input terminals;

wherein said second switch switches between a connection state of inputting an input signal from said at least one input terminal and a connection state of inputting a second predetermined voltage.

9. The semiconductor device as claimed in claim 7, said nonlinear element being an inverter circuit.

10. The semiconductor device as claimed in claim 8, said nonlinear element being an inverter circuit.

11. The semiconductor device as claimed in claim 9, said inverter circuit being a CMOS inverter or a resistive load type inverter.

12. The semiconductor device as claimed in claim 10, said inverter circuit being a CMOS inverter or a resistive load type inverter.

13. The semiconductor device as claimed in claim 5, each of said threshold elements comprising:

a semiconductor region of a first conductivity type disposed on a substrate;

a source region and a drain region of a second conductivity type provided on said semiconductor region;

a floating gate electrode provided on a region which separates said source region and said drain region via an insulating film, said floating gate electrode connected to a terminal having a first voltage via an element which can take a conducting state, and, an interrupted state or an electrically high impedance state;

a plurality of input gate electrodes connected to said floating gate electrode via an insulating film, said input gate electrodes controlled by at least two input control parts provided in said semiconductor device;

at least one element for switching which

can connects at least one of said input gate electrodes to an input line which inputs function configuration data or to a terminal having a second voltage.

14. A function reconfigurable integrated circuit, comprising:

a plurality of threshold elements;

each of said threshold elements including means which stores a threshold value; and

wherein a function which is realized by said integrated circuit is determined by determining said threshold value in each of said threshold elements.

15. The integrated circuit as claimed in claim 14, wherein said integrated circuit is configured by a plurality of stages, each of said stages including at least one threshold element.

16. The integrated circuit as claimed in claim 15, each of said threshold elements comprising:

a first input part which inputs an input signal to be processed;

a second input part which inputs a control signal for realizing said function;

wherein said threshold value is set by

said control signal, an output value for an input signal which is input from said first input part being determined according to said threshold value.

17. The integrated circuit as claimed in claim 15, each of said threshold elements comprising:

a plurality of input terminals;

a first terminal which can be regarded as an electrically insulated state transiently; and

a nonlinear element;

said input terminals being connected to said first terminal;

said nonlinear element receiving a voltage of said first terminal.

18. The integrated circuit as claimed in claim 17, each of said threshold elements further comprising:

a first switch between said first terminal and a terminal having a first predetermined voltage;

at least one second switch being connected to at least one input terminal in said input terminals;

wherein said second switch switches between a connection state of inputting an input signal from said at least one input terminal and a connection state of inputting a second predetermined voltage.

19. The integrated circuit as claimed in claim 17, said nonlinear element being an inverter circuit.

20. The integrated circuit as claimed in claim 18, said nonlinear element being an inverter circuit.

21. The integrated circuit as claimed in claim 19, said inverter circuit being a CMOS inverter or a resistive load type inverter.

22. The integrated circuit as claimed in claim 20, said inverter circuit being a CMOS inverter or a resistive load type inverter.

23. The integrated circuit as claimed in claim 15, each of said threshold elements comprising:

a semiconductor region of a first conductivity type disposed on a substrate;

a source region and a drain region of a second conductivity type provided on said

semiconductor region;

a floating gate electrode provided on a region which separates said source region and said drain region via an insulating film, said floating gate electrode connected to a terminal having a first voltage via an element which can take a conducting state, and, an interrupted state or an electrically high impedance state;

a plurality of input gate electrodes connected to said floating gate electrode via an insulating film, said input gate electrodes controlled by at least two input control parts provided in said semiconductor device;

at least one element for switching which can connects at least one of said input gate electrodes to an input line which inputs function configuration data or to a terminal having a second voltage.

24. A function reconfigurable integrated circuit, comprising:

neuron MOS transistors each of which includes a switch;

a circuit which stores function configuration data for determining a function as a vector which is a result of subtracting a third vector from the sum of a first vector and a second vector;

said first vector including, as elements, voltages of input gate electrodes of said neuron MOS transistors at a time when floating gate electrodes of said neuron MOS transistors are in a high impedance state or are interrupted from initialization terminals used for setting an initial

voltage in said floating gate electrode;

said second vector including, as elements, voltages of said floating gate electrodes at a time when said floating gate electrodes are connected to said initialization terminals;

said third vector including, as elements, voltages of said input gate electrodes at a time when said floating gate electrodes are interrupted from said initialization terminals or when said floating gate electrodes are in a high impedance state with respect to said initialization terminal.

25. The function reconfigurable integrated circuit as claimed in claim 24, said neuron MOS transistor comprising:

a semiconductor region of a first conductivity type disposed on a substrate;

a source region and a drain region of a second conductivity type provided on said semiconductor region;

said floating gate electrode, provided on a region which separates said source region and said drain region via an insulating film, said floating gate electrode connected to said initialization terminal having a predetermined voltage via an element which can take a conducting state, and, an interrupted state or an electrically high impedance state;

a plurality of input gate electrodes capacitively coupled to said floating gate electrode via an insulating film.

26. A function reconfigurable integrated circuit, comprising:

neuron MOS transistors each of which includes a switch;

a circuit which stores function configuration data for determining a function, said function configuration data being a difference between the sum of charge amounts induced in input gate electrodes of said neuron MOS transistors during performing a function processing and charge amounts of floating gate electrodes of said neuron MOS transistors at a time when said floating gate electrodes are interrupted from or become in a high impedance state with respect to an initialization terminal used for setting an initial voltage to said floating gate electrode.

27. The function reconfigurable integrated circuit as claimed in claim 26, said neuron MOS transistor comprising:

a semiconductor region of a first conductivity type disposed on a substrate;

a source region and a drain region of a second conductivity type provided on said semiconductor region;

said floating gate electrode, provided on a region which separates said source region and said drain region via an insulating film, said floating gate electrode connected to said initialization terminal having a predetermined voltage via an element which can take a conducting state, and, an interrupted state or an electrically high impedance state;

a plurality of input gate electrodes capacitively coupled to said floating gate electrode via an insulating film.

28. The function reconfigurable integrated circuit as claimed in claim 24, said integrated circuit including i input terminals, i being a positive integer, wherein;

when said function reconfigurable integrated circuit stores function configuration data including n elements, n being a positive integer, a time necessary for initialization of said floating gate electrodes is divided into j intervals on a time axis, j being a positive integer, such that $i+j \geqq n$ is satisfied, said time necessary for initialization being a time from a first time to a second time, at which said first time, at least one of said floating gate electrodes is connected to said initialization terminal, and at which said second time, said floating gate electrodes are interrupted from or enter in a high impedance state with respect to said initialization terminal; and

function configuration data is stored such that elements of said function configuration data are disposed on predetermined regions in a two dimensional plane which is formed by said i input terminals and said j intervals so as not to overlap one another.

29. The function reconfigurable integrated circuit as claimed in claim 26, said integrated

circuit including i input terminals, i being a positive integer, wherein;

when said reconfigurable integrated circuit stores function configuration data including n elements, n being a positive integer, a time necessary for initialization of said floating gate electrodes is divided into j intervals on a time axis, j being a positive integer, such that $i+j \geqq n$ is satisfied, said time necessary for initialization being a time from a first time to a second time, at which said first time, at least one of said floating gate electrodes being connected to said initialization terminal, at which said second time, said floating gate electrodes being interrupted from or becoming in a high impedance state with respect to said initialization terminal;

function configuration data is stored such that elements of said function configuration data are disposed on predetermined regions in a two dimensional plane which is formed by said i input terminals and said j intervals so as not to overlap one another.

30. The function reconfigurable integrated circuit as claimed in claim 24, further comprising:

a circuit which provides elements of said first vector as two-valued values of logical 1 or logical 0 or continuous values;

a circuit which provides elements of said second vector as two-valued values of logical 1 or logical 0 or continuous values; and

a circuit which provides elements of said third vector as two-valued values of logical 1 or logical 0 or continuous values.

31. The function reconfigurable integrated circuit as claimed in claim 24, wherein voltages which are provided from outside of said integrated circuit or voltages which are generated in said integrated circuit are used as elements of said first vector, said second vector and said third vector.

32. The function reconfigurable integrated circuit as claimed in claim 24, wherein said integrated circuit is configured by a plurality of stages, each of said stages includes at least one neuron MOS inverter having a switch which includes said neuron MOS transistor having a switch.

33. The function reconfigurable integrated circuit as claimed in claim 26, wherein said integrated circuit is configured by a plurality of stages, each of said stages includes at least one neuron MOS inverter having a switch which includes said neuron MOS transistor having a switch.

34. The function reconfigurable integrated circuit as claimed in claim 24, comprising:

a plurality of circuit blocks, each of said circuit blocks including at least one said integrated circuit;

wherein processing on storing function configuration data is performed in said integrated circuits simultaneously in each of said circuit blocks.

35. The function reconfigurable integrated circuit as claimed in claim 26, comprising:

a plurality of circuit blocks, each of said circuit blocks including at least one said integrated circuit;

wherein processing on storing function configuration data is performed in said integrated circuits simultaneously for each of said circuit blocks.

36. The function reconfigurable integrated circuit as claimed in claim 24, wherein:

multiple-valued voltages or continuous voltages are used for storing said function configuration data, said multiple-valued voltages or said continuous voltages being provided from the outside of said integrated circuit or being generated in said integrated circuit from voltages provided from the outside of said integrated circuit.

37. The function reconfigurable integrated circuit as claimed in claim 26, wherein:

multiple-valued voltages or continuous voltages are used for storing said function configuration data, said multiple-valued voltages or said continuous voltages being provided from the outside of said integrated circuit or being generated in said integrated circuit from voltages provided from the outside of said integrated circuit.

38. The function reconfigurable integrated circuit as claimed in claim 24, further comprising:

an impedance network which includes switches and impedance components; wherein,

said integrated circuit stores multiple-valued voltages or continuous voltages which are generated by said impedance network from voltages provided from the outside of said integrated circuit.

39. The function reconfigurable integrated circuit as claimed in claim 26, further comprising:

an impedance network which includes switches and impedance components; wherein,

said integrated circuit stores multiple-valued voltages or continuous voltages which are generated by said impedance network from voltages provided from the outside of said integrated circuit.

40. The function reconfigurable integrated circuit as claimed in claim 38, said impedance components connected in series between a first terminal and a second terminal which have different voltages; and

each of said switches being for connecting one of said impedance components to said input gate electrode of said neuron MOS transistor.

41. The function reconfigurable integrated circuit as claimed in claim 39, said impedance components connected in series between a first terminal and a second terminal which have different voltages; and

each of said switches being for connecting one of said impedance components to said input gate electrode of said neuron MOS transistor.

42. The function reconfigurable integrated circuit as claimed in claim 38, wherein said impedance network is configured such that capacitances are connected in parallel between a first terminal and a second terminal which have different voltages, each of said capacitances having a switch, and one of two terminals of each of said capacitances can be connected to one of said input gate electrodes of said neuron MOS transistors.

43. The function reconfigurable integrated circuit as claimed in claim 39, wherein said impedance network is configured such that capacitances are connected in parallel between a first terminal and a second terminal which have different voltages, each of said capacitances having a switch, and one of two terminals of each of said capacitances can be connected to one of said input gate electrodes of said neuron MOS transistor.

44. The function reconfigurable integrated circuit as claimed in claim 24, wherein said function configuration data is stored by storing charge amounts of multiple-valued values or charge amounts of continuous values, said multiple-valued values or said continuous values are represented by time intervals during which a predetermined voltage is provided, said predetermined voltage being provided from outside of said integrated circuit or being generated in said integrated circuit.

45. The function reconfigurable integrated circuit as claimed in claim 26, wherein said function configuration data is stored by storing charge amounts of multiple-valued values or charge amounts of continuous values, said multiple-valued values or said continuous values are represented by time intervals during which a predetermined voltage is provided, said predetermined voltage being provided from outside of said integrated circuit or being generated in said integrated circuit.

46. The function reconfigurable integrated circuit as claimed in claim 44, wherein said multiple-valued values or said continuous values are generated and stored by controlling said time intervals by using a network and a capacitance between said input gate electrode and said floating gate electrode, said network comprising resistance elements and capacitance elements and provided on a path over which a signal is applied to said input gate electrode.

47. The function reconfigurable integrated circuit as claimed in claim 45, said multiple-valued values or said continuous values are generated and stored by controlling said time intervals by using a network and a capacitance between said input gate electrode and said floating gate electrode, said network comprising resistance elements and capacitance elements and provided on a path over which a signal is applied to said input gate electrode.

48. A method of storing function configuration data in an integrated circuit including neuron MOS transistors each of which having a switch, said method comprising the steps of:

connecting each of floating gate electrodes of said neuron MOS transistors to an initialization terminal which is in a second voltage;

applying voltages in a third voltage vector to input gates of said neuron MOS transistors while each of said floating gate electrodes of said neuron MOS transistors is connected to said initialization terminal;

when a voltage of each of said floating gate electrodes can be regarded as the same as said second voltage, interrupting each of said floating gate electrodes from said initialization terminal or setting a high impedance with respect to said initialization terminal in each of said floating gate electrodes; and

applying voltages of a first voltage vector to said input gate electrodes.

49. A method of storing function configuration data in an integrated circuit including neuron MOS inverters each of which having a switch, said integrated circuit configured by a plurality of stages each of which stages including at least one of said neuron MOS inverters, wherein each of floating gate electrodes of said neuron MOS inverters can be connected to a ground terminal having a ground voltage via a switch, said method comprising the steps of:

when each of said floating gate electrodes is connected to said ground terminal, applying predetermined voltages to input gate electrodes of said neuron MOS inverters;

interrupting each of said floating gate

electrodes from said ground terminal or providing a high impedance to each of said floating gate electrodes while applying said predetermined voltages to said input gate electrodes;

when each of said floating gate electrodes can be regarded as in a floating state, applying a power supply voltage instead of said predetermined voltages to said input gate electrodes.

50. A method of storing function configuration data in an integrated circuit including neuron MOS inverters each of which having a switch, said integrated circuit configured by a plurality of stages each of which stages including at least one of said neuron MOS inverters, wherein each of floating gate electrodes of said neuron MOS inverters can be connected to a power supply terminal having a power supply voltage via a switch, said method comprising the steps of:

when each of said floating gate electrodes is connected to said power supply terminal, applying predetermined voltages to input gate electrodes of said neuron MOS inverters;

interrupting each of said floating gate electrodes from said power supply terminal or providing a high impedance to each of said floating gate electrodes while applying said predetermined voltages to said input gate electrodes;

when each of said floating gate electrodes can be regarded as in a floating state, applying a ground voltage instead of said predetermined voltages to said input gate electrodes.

51. A method of storing function configuration data in an integrated circuit including neuron MOS inverters each of which having a switch, said integrated circuit configured by a plurality of stages each of which stages including at least one of said neuron MOS inverters, wherein each of floating gate electrodes of said neuron MOS inverters can be connected to a second voltage terminal having a second voltage via a switch, said method comprising the steps of:

when each of said floating gate electrodes is connected to said second voltage terminal, applying third voltages to input gate electrodes of said neuron MOS inverters;

interrupting each of said floating gate electrodes from said second voltage terminal or providing a high impedance to each of said floating gate electrodes while applying said third voltages to said input gate electrodes;

when each of said floating gate electrodes can be regarded as in a floating state, applying a first voltage instead of said third voltages to said input gate electrodes.

52. An integrated circuit which realizes a function of k input variables, k being a positive integer, said integraated circuit comprising:

k first input signal terminals which input k first input signals and k+1 second input signal terminals which input k+1 second input signals, wherein input status numbers, each of which is the number of said first input signal terminals having

identical values, are in one-to-one correspondence with said second input signal terminals;

said integrated circuit outputting a value which is determined according to a state of said second input signal terminal which corresponds to said input status number;

said integrated circuit including a symmetric function capability of k input variables and a selector capability, said selector capability selecting one signal among said k+1 second input signals by using said k first input signals.

53. The integrated circuit as claimed in claim 52, comprising:

two stages, a first stage in said two stages including k+1 threshold elements, a second stage in said two stages including a threshold element;

each of said k+1 threshold elements in said first stage including terminals for inputting said k first input signals and a terminal for inputting one of said second input signals;

said threshold element in said second stage including terminals for inputting said k first input signals and terminals for inputting signals based on output signals of said k+1 threshold elements of said first stage;

each of said threshold elements in said first stage having a threshold value which is different from a threshold value of any other threshold element in said first stage;

said threshold element in said second stage receiving products of a first weight and signal values output from said k+1 threshold

elements of said first stage, said first weight having reversed sign of a second weight by which said first input signals are multiplied, or said threshold element in said second stage receiving products of a positive weight and reversed signals of signals output from said k+1 threshold elements of said first stage.

54. A function reconfigurable integrated circuit comprising at least one neuron MOS transistors having a switch;

said neuron MOS transistor including an element between a floating gate electrode and a terminal of a predetermined voltage, wherein said element can take either of two states of a conducting state and an interrupted state or a high impedance state; wherein,

said integrated circuit has a symmetric function capability and a selector capability by controlling at least one of three voltages, a first voltage of said three voltages being a voltage of said floating gate electrode at a time when said element is in said conducting state, a second voltage of said three voltages being a voltage of an input terminal of said neuron MOS transistor at a time when said element is in said conducting state, a third voltage of said three voltages being a voltage of said input terminal of said neuron MOS transistor at a time when said element is in said interrupted state.

55. The function reconfigurable integrated circuit as claimed in claim 54, said neuron MOS transistor comprising:

a semiconductor region of a first conductivity type disposed on a substrate;

a source region and a drain region of a second conductivity type provided on said semiconductor region;

said floating gate electrode, which can be regarded as in a floating state, provided on a region which separates said source region and said drain region via an insulating film, said floating gate electrode connected to said terminal having a predetermined voltage via said element;

a plurality of input gate electrodes capacitively coupled to said floating gate electrode via an insulating film.

56. The function reconfigurable integrated circuit as claimed in claim 54, comprising:

two stages, a first stage in said two stages including k+1 threshold elements using said neuron MOS transistors, a second stage in said two stages including a threshold element using said neuron MOS transistor;

each of said k+1 threshold elements in said first stage including k first input signal terminals, a second input signal terminal which is different from other second input signal terminals of other threshold elements;

said threshold element in said second stage including terminals for inputting k first input signals and k+1 terminals for inputting signals based on output signals of said k+1

threshold elements of said first stage;

each of said threshold elements in said first stage having a threshold value which is different from a threshold value of any other threshold element in said first stage;

said threshold element in said second stage receiving products of a positive weight and reversed signals of signals output from said k+1 threshold elements of said first stage.

57. The function reconfigurable integrated circuit as claimed in claim 54, further comprising a switching circuit which selects between said symmetric function capability and said selector capability.

58. The function reconfigurable integrated circuit as claimed in claim 54, further comprising a control circuit which switches between four modes;

in a first mode, said symmetric function capability being realized only during applying function configuration data ;

in a second mode, said function configuration data being stored;

in a third mode, said selector capability being realized only during applying an address of a signal to be selected;

in a fourth mode, said address being stored.

59. The function reconfigurable integrated circuit as claimed in claim 54, said function reconfigurable integrated circuit comprising threshold elements using said neuron MOS transistor having a switch which forms an inverter circuit.

60. The function reconfigurable integrated circuit as claimed in claim 56, said threshold element using said neuron MOS transistor having a switch being an element which forms an inverter circuit.

61. The function reconfigurable integrated circuit as claimed in claim 56, wherein output terminals of said threshold elements of said first stage are connected to input terminals of said threshold element of said second stage via circuits including wave-shaping circuits.

62. The function reconfigurable integrated circuit as claimed in claim 56, further comprising a circuit including a delay circuit, which is provided on a path over which a signal is applied to said threshold element of said second stage.

63. A function reconfigurable integrated circuit which includes a plurality of neuron MOS transistors or a plurality of neuron MOS transistors having a switch, wherein said integrated circuit is configured such that:

sums of sets of an element or elements are different with respect to each other, wherein said elements in a set do not overlap each other, said elements being included in a capacitance ratio set $(W_1, W_2, \cdots, W_i, \cdots, W_k)$;

wherein each element in said capacitance ratio set $(W_1, W_2, \cdots, W_i, \cdots, W_k)$ is a capacitance ratio with respect to a minimum value of capacitance values, said capacitance values being values of capacitances between input gate electrodes to which input variables are input and a floating gate electrode, wherein k is the number of said input variables.

64. The function reconfigurable integrated circuit as claimed in claim 63, each of said neuron MOS transistor and said neuron MOS transistor having a switch comprising:

a semiconductor region of a first conductivity type disposed on a substrate;

a source region and a drain region of a second conductivity type provided on said semiconductor region;

said floating gate electrode, which can be regarded as in a floating state, provided on a region which separates said source region and said

drain region via an insulating film;

a plurality of input gate electrodes capacitively coupled to said floating gate electrode via an insulating film;

wherein said floating gate electrode of said neuron MOS transistor having a switch is connected to a terminal having a predetermined voltage via an element which can take either of a conducting state and an interrupted state or a high impedance state.

65. The function reconfigurable integrated circuit as claimed in claim 63, each of said neuron MOS transistor and said neuron MOS transistor having a switch being a transistor wherein said capacitance ratio w_i of an ith input gate satisfies $w_i > \sum_{j=1}^{i-1} w_j, (2 \leqq i \leqq k)$.

66. The function reconfigurable integrated circuit as claimed in claim 65, each of said neuron MOS transistor and said neuron MOS transistor having a switch being a transistor wherein $w_i = z^{i-1}$, $1 \leqq i \leqq k$, and $z \geqq 2$ are satisfied.

67. The function reconfigurable integrated circuit as claimed in claim 63, each of said neuron MOS transistor and said neuron MOS transistor having

a switch being a transistor wherein $w_i = \alpha^{i-1}$, $1 \leqq i \leqq k$ and $1 < \alpha < 2$ are satisfied.

68. The function reconfigurable integrated circuit as claimed in claim 65, each of said neuron MOS transistor and said neuron MOS transistor having a switch being a transistor wherein $w_i = \alpha^{i-2} \cdot (1+\beta)$, $2 \leqq i \leqq k$, $\alpha > 1$ and $0 < \beta < 1$ are satisfied.

69. The function reconfigurable integrated circuit as claimed in claim 68, each of said neuron MOS transistor and said neuron MOS transistor having a switch being a transistor wherein $w_i = 2^{i-2} \cdot (1+\beta)$, $2 \leqq i \leqq k$ and $0 < \beta < 1$ are satisfied.

70. The function reconfigurable integrated circuit as claimed in claim 63, said integrated circuit including two stages, a first stage of said two stages including pre-inverters each of which is said neuron MOS transistor or said neuron MOS transistor having a switch, said pre-inverter having more than two threshold values with respect to an input signal.

71. The function reconfigurable integrated

circuit as claimed in claim 70, further comprising terminals from which two-valued control signals which determine said threshold value are input.

72. The function reconfigurable integrated circuit as claimed in claim 70, further comprising a control signal terminal from which a multiple-valued signal or an analog signal is input, said multiple-valued signal or said analog signal determining said more than two threshold values.

73. A designing method of a function reconfigurable integrated circuit, said integrated circuit comprising two stages which include neuron MOS inverters using neuron MOS transistors or neuron MOS transistors having a switch, said neuron MOS inverter in a first stage of said two stages being a pre-inverter and said neuron MOS inverter in a second stage of said two stage being a main inverter, said method comprising the steps of:

setting values of input gate capacitances, for each of said neuron MOS inverters, between input gate electrodes from which first input signals are input and a floating gate electrode such that input vectors can be identified, said input vector being a vector representation of said first input signals;

setting, for each input gate electrode connected to an output terminal of said pre-inverter, a value of an input gate capacitance between an input gate electrode from which an output signal from a pre-inverter is input and said floating gate

of said main inverter such that, of two different voltages of said floating gate which correspond to two output values of said pre-inverter, one is larger than a threshold voltage of said floating gate and another is smaller than said threshold voltage, wherein said input gate capacitance corresponds to said pre-inverter which corresponds to one of said input vectors; and

setting, for each of said pre-inverters, a value of an input gate capacitance between an input gate electrode from which a second input signal is input and said floating gate of one of said pre-inverters, such that a voltage of said floating gate becomes equal to said threshold voltage at each of two different input charge amounts, wherein an input charge amount corresponding to said one of said pre-inverters which corresponds to a first input vector is larger than one of said two different input charge amounts and is smaller than the other of said two different input charge amounts, wherein each of said two different input charge amounts does not exceed an input charge amount of a second input vector which is nearest to said first input vector.

74. A designing method of a function reconfigurable integrated circuit, said integrated circuit comprising two stages which include neuron MOS inverters using neuron MOS transistors or neuron MOS transistors having a switch, said neuron MOS inverter in a first stage of said two stages being a pre-inverter and neuron MOS inverter in a second stage of said two stages being a main inverter, said method comprising the steps of:

setting values of input gate capacitances,

for each of said neuron MOS inverters, between input gate electrodes from which first input signals are input and a floating gate electrode, such that input vectors can be identified, said input vector being a vector representation of said first input signals;

for said main inverter, dividing said input vectors which are arranged in ascending order by corresponding input charge amounts into blocks each of which blocks including four input vectors, said input charge amounts being accumulated in input gate capacitances between first input signal terminals and a floating gate;

setting values of input gate capacitances, for said main inverter, between input gate electrodes from which output signals from said pre-inverters are input and said floating gate, such that said floating gate takes two values of which one is larger than a threshold voltage of said floating gate and another is smaller than said threshold voltage of said floating gate by using combinations of logical values of output signals of three pre-inverters for four input vectors in said block; and

setting, for each of said pre-inverters, a value of an input gate capacitance between an input gate electrode from which a second input signal is input and said floating gate of one of said pre-inverters, such that a voltage of said floating gate becomes equal to said threshold voltage at each of two different input charge amounts, wherein an input charge amount corresponding to said one of said pre-inverters which corresponds to a first input vector is larger than one of said two different input charge amounts and is smaller than another of said two different input charge amounts, wherein each of said two different input charge amounts does not exceed an input charge amount of a second input

vector which is nearest to said first input vector.

75. The designing method of a function reconfigurable integrated circuit as claimed in claim 74, further comprising the step of utilizing a physical multiple-valued value for a multiple-valued expression.